Transport properties of InAs nanowire field effect transistors: The effects of surface states

Shadi A. Dayeh, Cesare Soci, Paul K. L. Yu, Edward T. Yu,[a] and Deli Wang[b]
Department of Electrical and Computer Engineering, University of California, San Diego, 9500 Gilman Drive, Mail Code 0407, La Jolla, California 92093-0407

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It is shown that interface trap states have pronounced effects on carrier transport and parameter extraction from top-gated InAs nanowire field effect transistors (NWFETs). Due to slow surface state charging and discharging, the NWFET characteristics are time dependent with time constants as long as ~45 s. This is also manifested in a time-dependent extrinsic transconductance that severely affects carrier mobility and carrier density determination from conventional three-terminal current-voltage characteristics. Slow gate voltage sweep rates result in charge balance between carrier capture and emission from interface states and lead to reduced hysteresis in the transfer curves. The gate transconductance is thus increased and intrinsic NW transport parameters can be isolated. In the InAs NWFETs, a carrier mobility value of ~16 000 cm^2/V s was obtained from the transfer curves at slow sweep rates, which is significantly higher than ~1000 cm^2/V s obtained at fast sweep rates. A circuit model that takes into account the reduction in the extrinsic transconductance is used to estimate an interface state capacitance to be ~2 $\mu F/cm^{-2}$, a significant value that can lead to underestimation of carrier mobility. © *2007 American Vacuum Society.* [DOI: 10.1116/1.2748410]

I. INTRODUCTION

Due to their unique electronic and optical properties, semiconductor nanowires have been the subject of extensive research as potential building blocks for a variety of electronic,[1] photonic,[2] and biomedical[3] applications. Because of the high surface area to volume ratio in nanoscale devices, surface effects become important, and even dominant, in their influence on electronic transport[4] and optical behavior.[5] While these effects can be desirable in some applications such as highly sensitive photodetectors[6] or chemical and biological sensors,[7] they may be detrimental to carrier transport properties in nanowire field effect transistors (NWFETs).[8]

In order to obtain accurate and representative measures of transport properties in NWFETs, the capacitive effects of interface states must be considered. While traditional capacitance-voltage (*C-V*) measurements can offer detailed information concerning the presence, nature, and density of interface trap states,[9] these techniques are not readily applicable to NWFETs due to their small gate capacitance. Herein, we report studies on the influence of interface states on the transport properties and parameter extraction from top-gated InAs NWFETs carried out by steady state and time-resolved *I-V* measurements.

Our efforts focus on InAs NWFETs, which are promising for high speed nanoelectronics due to their high electron mobility and ability to form low resistance Ohmic contacts[4] (~1–10 kΩ) due to surface Fermi energy pinning in the conduction band.[10] Surface Fermi level pinning in InAs is caused by surface reconstruction[11] and by the abundance of donor-type surface states.[12] Therefore, it is expected that the effects of surface states will be highly pronounced in this material system. Indeed, as discussed in the following, the InAs NWFETs show marked transient characteristics and sweep rate dependent transconductance. By performing a systematic characterization of the transport properties of InAs NWFETs as well as an equivalent circuit analysis, we are able to model and quantify their transport properties and extract transport parameters reflective of the inherent properties of the nanowires.

II. EXPERIMENT

InAs NWs were grown by metal-organic chemical vapor deposition. 40 nm Au colloids were dispersed on thermally grown SiO_2 on Si(001) and the growth was performed at a substrate temperature of 350 °C under 100 Torr chamber pressure using trimethylindium and arsine in H_2 carrier gas at an input V/III ratio of 50 for 13–30 min. The resulting NWs are *n* type and have diameters of 60–120 nm and lengths of ~10 μm. The nanowires were then suspended in ethanol solution and transferred onto a prepatterned grid on a 600 nm SiO_2/n^+-Si(001) substrates for device fabrication and characterization.

Source-drain contact leads with a variable separation of ~0.5–4 μm were patterned by e-beam lithography and e-beam evaporation of Ti/Al (15/90 nm) followed by lift-off. A 73 nm ZrO_2/Y_2O_3 gate dielectric (ε_r=12) layer was then rf sputtered, and e-beam lithography and bilayer lift-off were then performed to pattern the 100 nm thick Al top gate, which was also deposited by rf sputtering. Figure 1 shows a field-emission scanning electron microscope (FE-SEM) image of the final top-gate InAs NWFET device. The transfer curves were measured using an HP4155 parameter analyzer and the transient characteristics were measured using a com-

[a]Electronic mail: ety@ece.ucsd.edu
[b]Electronic mail: dwang@ece.ucsd.edu

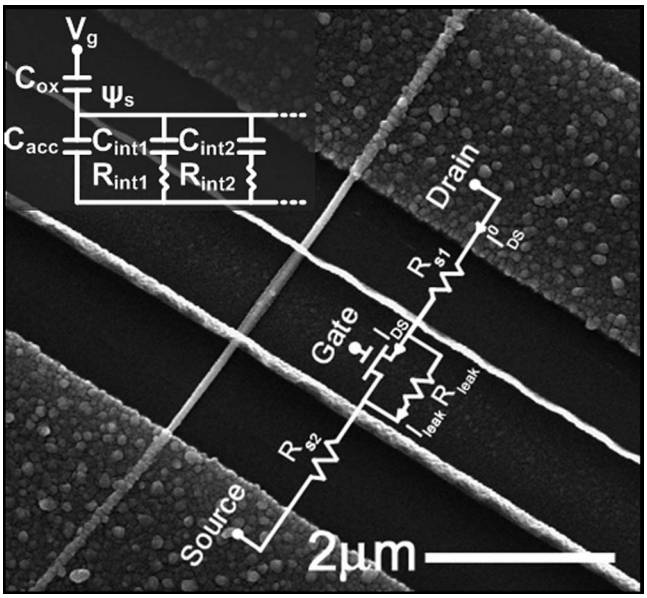

FIG. 1. FE-SEM image of InAs NWs grown on SiO_2 substrates. Top inset is the equivalent capacitance circuit where C_{int} and R_{int} are associated with the interface trap density. Bottom inset is equivalent dc circuit model for the underlap top-gate NWFET.

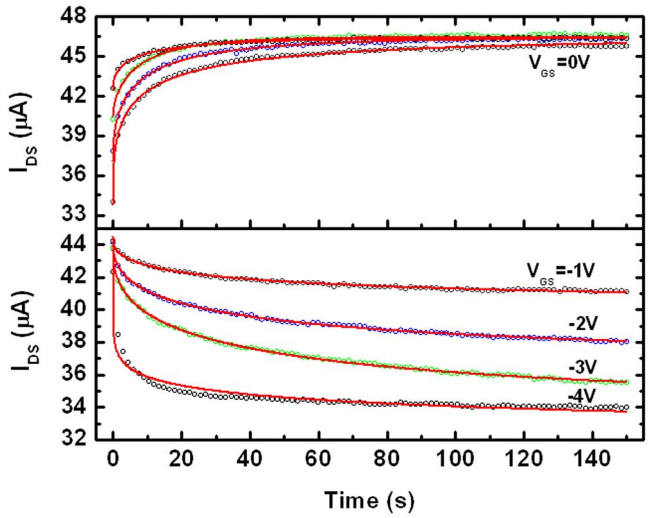

FIG. 2. Time-resolved transfer characteristics of an InAs NWFET with $L_{SD}=3.35$ μm, $L_G=1.02$ μm, and $D=72$ nm, showing long characteristic time constants up to 45 s (open circles) and stretched exponential fits to these curves (solid lines).

puterized data acquisition board (National Instruments PCI-6030E, 100 kS/s), a current preamplifier (Ithaco 1211), and a voltage source (Keithley 6487).

III. RESULTS AND DISCUSSION

In order to extract transport parameters such as carrier mobility and carrier density from the top-gate InAs NWFET device shown in Fig. 1, one has to take into account parasitic circuit components characteristic of the device geometry, as shown in the bottom inset to Fig. 1.[4] The dc equivalent circuit model consists of drain (R_{s1}) and source (R_{s2}) extension and contact resistances, and a leakage resistance R_{leak} which accounts for the unmodulated portion of the NWFET device. The equivalent capacitance model shown in the top inset of Fig. 1 includes the oxide capacitance C_{ox}, an accumulation capacitance per unit area $C_{acc}(\Psi_s)$, an interface state capacitance per unit area $C_{int}(\Psi_s)$, and resistance R_{int} which in combination account for interface trap states with characteristic time constant $\tau_{int}=AR_{int}C_{int}$, A is the gate area.[13] Ψ_s is the oxide-InAs surface potential. A detailed circuit analysis taking into account these parasitic components yields an expression for the field effect mobility (μ_{FE}) as a function of the applied and measured quantities across the three physical device electrodes:[4]

$$\mu_{FE}=\frac{L_G^2 V_{DS}^0(1+C_{int}/C_{acc})/C_{ox}}{[[(V_{DS}^0-V_s)^2/g_m^0]-V_s^2R_{s2}-V_{DS}^0R_{s2}(V_{DS}^0-2V_s)]}, \quad (1)$$

where L_G is the gate length, V_{DS}^0 is the applied source-drain voltage, $g_m^0 \equiv dI_{DS}^0/dV_{GS}^0$ is the extrinsic transconductance, and V_s is the voltage drop across R_{s1} and R_{s2}. An increased interface state density results in an increase in the interface state capacitance and a corresponding reduction of the equivalent gate capacitance, $C_G=C_{ox}/(1+C_{int}/C_{acc})$. As a result, extraction of the field effect mobility without considering the interface state capacitance results in underestimated mobility values, as evident from Eq. (1).

The interface state capacitance can be expressed as[13]

$$C_{int}=\frac{dQ_{int}}{d\Psi_s}=q\frac{dn_{int}}{dE_s} \quad (\mathrm{F/cm^{-2}}), \quad (2)$$

where Ψ_s and E_s are the surface potential and energy at the gate oxide-semiconductor interface, respectively, Q_{int} is the modulated interface charge density in the gate area A, and n_{int} is the surface state density. Ψ_s is a function of both the axial and the radial potential drops across the device. Thus, C_{int} is a differential capacitance which is a function of Ψ_s and is subject to change while measuring the device output and transfer curves. Substantial errors might arise in calculation of μ_{FE} from Eq. (1) if one assumes a single numerical value for C_{int}. Measurements of the transfer curves where the interface charge density is modulated or reduced (by varying the gate voltage sweep rate) are therefore utilized to reveal the effects of C_{int} on electrical characteristics and parameter extraction.

Figure 2 shows transient transfer curves measured at constant $V_{DS}=0.5$ V and various V_{GS} values held for 150 s each with V_{GS} switched in the following sequence: 0 V, −4 V, 0 V, +4 V, 0 V, …, −1 V, 0 V, +1 V, 0 V. The transient decays were fitted using a stretched exponential rise and decay of the form

$$I=I_\infty+(I_0-I_\infty)\exp(-t/\tau)^\alpha, \quad (3)$$

where I_0 and I_∞ are the initial and final values of the source-drain current when the interface states are populated (charge neutral) and empty (positively charged), respectively, τ is the surface state trapping and detrapping time constant, and $\alpha(0<\alpha<1)$ is the stretching parameter.[14] 1-α indicates the strength of the driving force which determines the change in

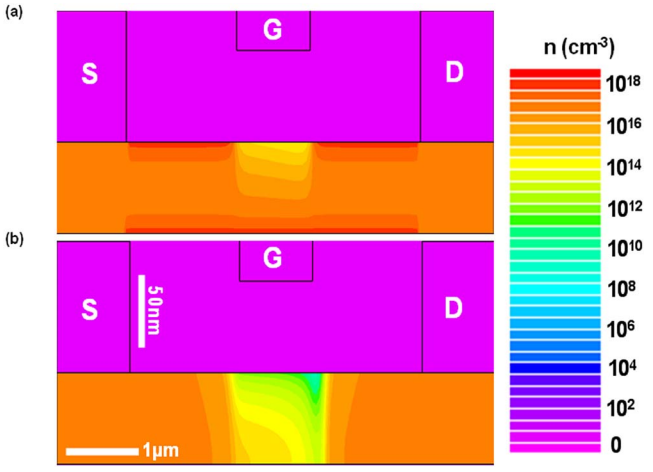

FIG. 3. 2D Silvaco Atlas simulation of the carrier concentration for a 70 nm diameter InAs NWFET ($N_D=5\times10^{16}$ cm^{-3}) with (a) fixed positive charged traps ($q_f=10^{12}$ cm^{-2}) under the gate and (b) charge neutral surface under the gate. $V_{DS}=0.5$ V and $V_{GS}=-2$ V.

current rise or decay rates with time. This force changes with time due to surface state trapping and detrapping that affects the current rise and decay rates k, where $dI/dt=-k(t)I(t)$, $k(t)\propto t^{\alpha-1}$. From the curves fitted to the data in Fig. 2 using Eq. (3), α decreases from 0.64 to 0.15 as V_{GS} is reduced from -1 to -4 V. At -4 V, the larger electrostatic fields at the oxide-InAs interface produce faster change of the decay rates as time progresses when compared to the smaller fields at $V_{GS}=-1$ V.

Interface trap states for InAs are known to have donor-type characteristics,[15] i.e., are charge neutral when occupied by an electron and positively charged otherwise.[16] As the surface state density increases, the localized states can begin to overlap, forming a "surface band" through which conduction may occur.[17] Thus, turning off the channel of the NWFET can require depleting the surface band and overcoming the resulting positively charged states. When negative V_{GS} is applied, positively charged surface states at the InAs surface (Q_{int}) reduce the gate field by Q_{int}/ε_{ox} and the gate voltage by $Q_{int}t_{ox}/\varepsilon_{ox}$, where t_{ox} and ε_{ox} are the oxide thickness and dielectric constant, respectively. This will reduce full depletion of the NWFET channel. To confirm the latter behavior, we have performed two-dimensional (2D) Silvaco Atlas simulations for a device structure similar to the fabricated one. Contour maps of the carrier concentration for $V_{GS}=-2$ V and $V_{DS}=0.5$ V are shown in Fig. 3. In the presence of a fixed positive charge ($q_f=10^{12}$ cm^{-2}) (Ref. 18) at the NW surface, an accumulation layer of electrons is formed at the surface and the depletion region extends only a small distance under the gate, as shown in Fig. 3(a). For the same device structure and same applied voltages, but without the fixed positive charge, the depletion width extends further into the channel, as shown in Fig. 3(b). From Fig. 3(a), we see that even if the surface conduction channel associated with the surface band is turned off, the presence of positive charges prevents full NW channel depletion leading to high off-state currents.

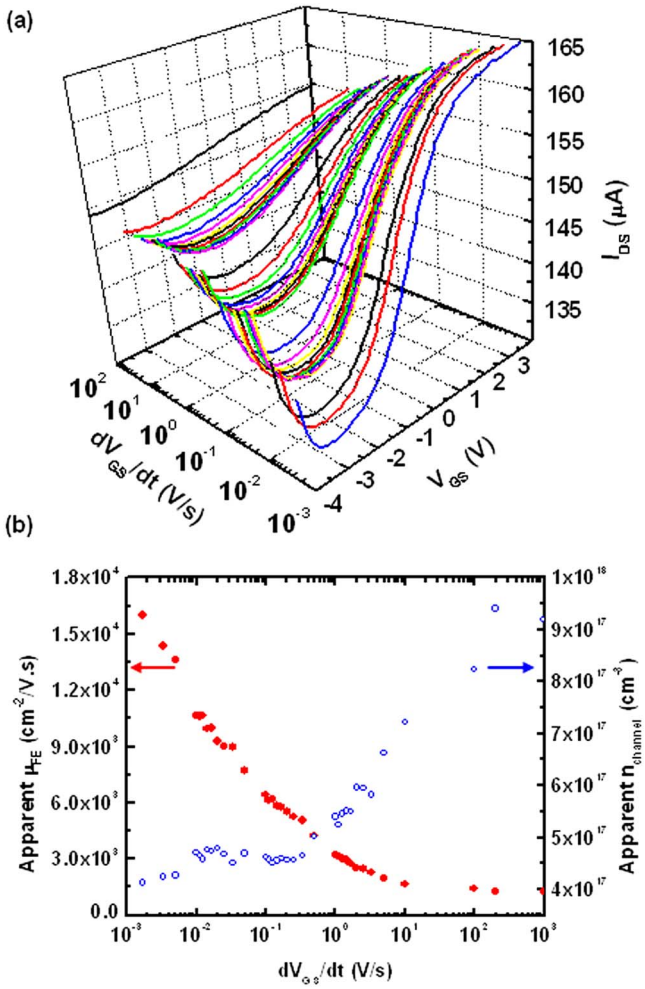

FIG. 4. (a) Transfer curves of an InAs NWFET with $L_{SD}=3.5$ μm, $L_G=0.78$ μm, and $D=110$ nm, plotted for different gate voltage sweep rates. (b) Computed μ_{FE} and $n_{channel}$ from the transfer curves in (a).

Figure 4(a) shows a set of sweep rate dependent transfer curves with negative to positive sweep direction obtained with $V_{DS}=0.5$ V. Slow V_{GS} sweep rates allow interface state charging and discharging to follow the sweep rate and minimize the interface state capacitance resulting in higher transconductance. The extrinsic transconductance varies by more than one order of magnitude (1–12 μS) when the sweep rate is varied from 10^3 V/s to 1.7 mV/s. Moreover, for slower sweep rates (i.e., when $qd\psi_s/dt\leq E_{trap}/\tau$), I_{DS} exhibits evident decay in the off-state biasing region. This is a consequence of a long detrapping time constant which causes the apparent "tail" in the I_{DS}-V_{GS} characteristics seen in Fig. 4(a). The highest measured gate leakage current was six orders of magnitude less than that of the source-drain current and thus, gate leakage current has no effect on the observed I_{DS} tails. For such devices with high turn off currents, the onset gate voltage for current modulation in the NW segment under the gate can be defined as the threshold voltage V_T. Once $V_{GS}\geq V_T$, the gate transconductance overcomes the current decay and I_{DS} increases with increasing V_{GS}. An increase in the transconductance implies a higher measured carrier mobility, as seen from Eq. (1). Figure 4(b) shows the

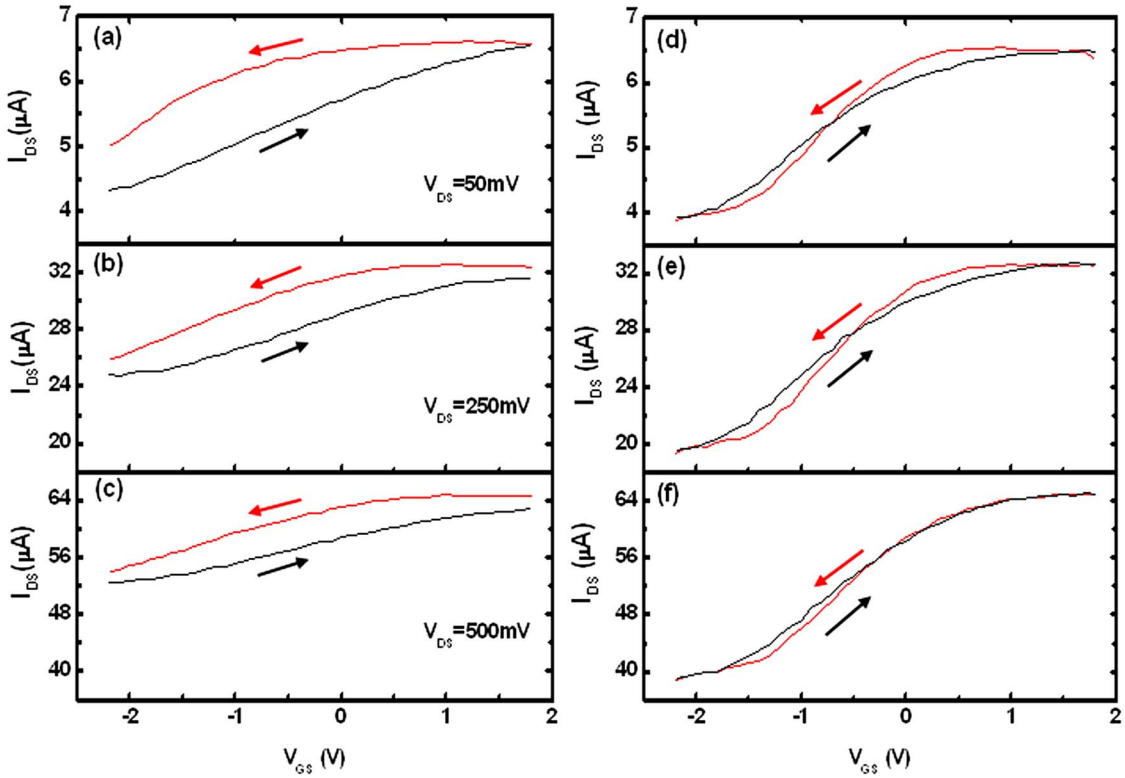

FIG. 5. I_{DS}-V_{GS} for an InAs NWFET device with L_{SD}=1.85 μm, L_G=585 nm, and D=63 nm. [(a)–(c)] Hysteresis plots for fast gate voltage sweep rate >10 V/s. [(d)–(f)]. Hysteresis plots with a slower gate voltage sweep rate of 6.7 mV/s.

computed apparent mobility values from the transfer curves using Eq. (1) where C_{int}/C_{acc} was set to zero. Mobility values of ~1000 $cm^2/V\,s$ extracted using this technique from these InAs NWFETs with fast V_{GS} sweep rates are in good agreement with those reported for similar InAs NW devices.[19,20] For slow V_{GS} sweep rates, much higher field effect mobility value (16 000 $cm^2/V\,s$) is obtained and is suggestive of the potential of InAs NWs for high speed nanoelectronics provided that the necessary surface passivation is achieved.

Similarly, the effects of interface states on the charge carrier density in the channel are non-negligible. One can compute the channel charge from the extracted I_{DS}-V_{GS} characteristics for the NW portion under the gate using $n_{channel} = I_{DS}L_G/q\mu_{FE}V_{DS}A$, where μ_{FE} as obtained from Eq. (1) accounts for the effect of interface states. Figure 4(b) shows the extracted carrier densities for this NWFET with different V_{GS} sweep rates. Slow V_{GS} sweep rate results in greater depletion width and consequently reduction in the carrier concentration under the gate as discussed earlier and is consistent with the extracted carrier concentration values. This is opposite to what is observed in, for example, GaN/AlGaN-based Heterojunction FETs, where the negative interface state charge in the gate-drain extension region acts as a surface virtual gate and causes further depletion of the channel.[21] Interface state charging in the extension regions for this InAs NWFET has not been considered in this analysis due to its minimal effects when V_{DS} is held constant. The potential drop differences in these extension regions would be insignificant between successive measurements. Interface state charge modulation is expected to be higher directly beneath the top gate due to the rapid decay of the gate field in the extension regions, as can be seen in Fig. 3(a).

Figures 5(a)–5(c) show the transfer curves obtained with a V_{GS} sweep rate >10 V/s in both directions at V_{DS}=50 mV, 250 mV, and 500 mV, respectively, revealing clear hysteresis. With a slow sweep rate of 6.7 mV/s, hysteresis in the transfer curves is diminished for all V_{DS} values, as shown in Figs. 5(d)–5(f). This indicates that surface state modulation occurs mostly under the gate in these InAs NWFETs because reduction in hysteresis prevails for all V_{DS} values. Also, the "off" current levels at negative V_{GS} for slower sweep rates are lower than those obtained with fast sweep rates. Hysteresis that arises from surface-related mechanisms, due to time lags between capture and emission from interface states, can be reduced by surface passivation.[22,23] However, the possibility of mobile ion drift in the oxide cannot be excluded when explaining the observed hysteresis. Ion-drift-type hysteresis is typically observed and quantified from oxide C-V measurements not readily available for NWs.[24] Since the gate leakage current in these devices is negligible, oxide and mobile charges were not included in our analysis. The reduction in the hysteresis plots through the measurement technique we present here indicates a charge balance between surface state trapping and detrapping and implies that our measurements with reduced sweep rates yield transport parameters for the InAs NWFET channel that reflect more accurately the inherent transport behavior in the NW.

Using an equivalent circuit model for the NWFET as shown in Fig. 1,[4,25] one can also estimate the interface state capacitance contributing to the hysteresis shown in Fig. 5, by quantifying its effects on the intrinsic transconductance. In the presence of interface state modulation, the current in the NW portion under the gate can be expressed as[4]

$$I_{DS} = \mu_{FE}[C_{ox}/(1 + C_{int}/C_{acc})](V_{GS} - V_T)V_{DS}/L_G^2. \quad (4)$$

The intrinsic transconductance can then be calculated from Eq. (4) to be

$$g_{m1} = \mu_{FE}\frac{C_{ox}}{1 + C_{int}/C_{acc}}\frac{V_{DS}}{L_G^2}. \quad (5)$$

When interface state capture and emission processes are balanced, I_{DS} can be expressed in the form

$$I_{DS} = \mu_{FE}C_{ox}(V_{GS} - V_T)V_{DS}/L_G^2, \quad (6)$$

due to the elimination of C_{int}. The expression for intrinsic transconductance in this case reverts to its more usual form

$$g_{m2} = \mu_{FE}C_{ox}\frac{V_{DS}}{L_G^2}. \quad (7)$$

Note that for each measurement at a fixed sweep rate, there is a shift in the threshold voltage. However, this does not alter Eq. (7) which represents the slope of I_{DS}-V_{GS} that is independent of V_T shift.

The ratio of the transconductances in Eqs. (5) and (7) can then be written as

$$g_{m2}/g_{m1} = 1 + \frac{C_{int}}{C_{acc}}. \quad (8)$$

Equation (8) quantifies the contribution of C_{int} to the extrinsic transconductance and relates its variation with V_{GS} sweep rates as shown in Fig. 4(a) due to the variation of C_{int}.

With a slow sweep rate of 6.7 mV/s, hysteresis in the transfer curves was greatly diminished due to the charge balance between trapping and detrapping of interface states. In this case, Eq. (7) provides an adequate description of the intrinsic transconductance. For faster sweep rates, the intrinsic transconductance is described by Eq. (5). The interface state capacitance can then be obtained from Eq. (8). The ratio of the intrinsic transconductance extracted from the transfer curves of Figs. 5(c) and 5(f) is g_{m1}/g_{m2}=35.4 μS/15.3 μS =2.3. From a one-dimensional Schrödinger-Poisson solution using Silvaco Atlas[26] for a planar structure similar to that of the InAs NWFET used in this study, an ~10 nm spatial separation of the accumulation charges from the interface was computed. Equation (8) can then be used to estimate the interface state capacitance to be ~2 μF/cm^{-2} which is a non-negligible quantity compared to C_{acc} and leads to mobility under estimation if not considered, as can be seen from Eq. (1).

IV. CONCLUSION

In summary, we have fabricated top-gated InAs NWFETs and analyzed the capacitive effects of surface states on their transport properties. Through detailed device and circuit analysis, we presented techniques that enable modeling and prediction of surface state effects on transport properties including transient behavior, sweep rate dependent transconductance, and hysteresis in transfer curves. Our analysis suggests that measurements with slow gate voltage sweep rates yield transport properties of the NWFETs most representative of the inherent behavior of the NW. The high mobility value obtained from this analysis (16 000 cm^2/V s) highlights the potential of utilizing surface-passivated InAs NWs for high speed nanoelectronic applications.

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