Influence of surface states on the extraction of transport parameters from InAs nanowire field effect transistors

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The capacitive effects of interface trap states in top-gated InAs nanowire field effect transistors and their influence on the experimental extraction of transport parameters are discussed. Time resolved transfer characteristics exhibit transient behavior indicating surface state trapping and detrapping with long characteristic time constants of 45 s. Varying gate voltage sweep rate results in a time-dependent extrinsic transconductance; a reduced gate voltage sweep rate leads to a charge neutral interface, reduced interface state capacitance, higher measured transconductance, and minimal hysteresis. These results demonstrate that measurements with a charge neutralized or passivated surface are key to extract intrinsic nanowire transport parameters. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2728762]

Semiconductor nanowires (NWs) have attracted intense research interest due to their potential applications in electronic and photonic devices and integrated functional systems.[1–3] InAs NWs are of particular interest for potential high-speed nanoelectronic applications due to their high electron mobilities.[4–6] However, the electronic[7,8] and optoelectronic properties[9] of NW devices are dramatically affected by surface and interface states due to their large surface area to volume ratio. While these effects can be desirable in some applications such as highly sensitive photodetectors,[10] chemical and biological sensors,[11] they may be detrimental for transport properties of nanowire field-effect transistors (NWFETs).[4] Thus, understanding and quantifying the effects of surface states is necessary to accurately assess the intrinsic NW parameters and to enable control over and optimization of NW device performance.

In this letter, we present an investigation of the capacitive effects of surface states on the analysis of transport properties of InAs NWFETs, where (1) the transfer characteristics of the NWFETs are strongly dependent on gate voltage sweep rate; (2) the hysteresis in the transfer characteristics can be minimized and eliminated by reducing the gate voltage sweep rate, suggesting that slow sweep rates yield measurements that are most representative of the intrinsic nanowire carrier transport behavior; and (3) a circuit model analysis by including the effects of the interface state capacitance and the intrinsic transconductance is developed to analyze the transport behavior.

InAs NWs for these studies, with diameters of 60–120 nm and lengths of $\sim$10 μm, were grown by metal-organic chemical vapor deposition on a SiO_2/Si substrate with V/III ratio of 50 at 350 °C and the top-gated NWFETs were fabricated on 600 nm SiO_2/n^+-Si utilizing e-beam lithography for Ti/Al source-drain contact leads and Al top gate patterning.[4] A 73 nm rf sputtered ZrO_2/Y_2O_3 layer extending over the source-drain contacts served as a gate dielectric. The Ti/Al contact results in a low Ohmic contact resistance of 1–10 kΩ[4] due to surface Fermi energy pinning and electron accumulation at the InAs surface.[12,13] As a conservative estimate, a low contact resistance (which maximizes resistance attributed to the NW) of 1 kΩ has been used for parameter extraction.

Figure 1(a) shows a schematic diagram of a top-gated InAs NWFET device with an equivalent circuit consisting of series resistances to account for the drain (R_{s1}) and source (R_{s2}) contact and extension resistances, and a leakage resistance R_{leak} to account for the unmodulated portion of the NWFET device. Interface states contribute to an interface trap capacitance C_{int},[14] parallel to the accumulation capacitance C_{acc} as depicted in the enlarged inset of Fig. 1(a). The depletion capacitance is not considered in this scheme because the devices are operated in depletion mode. By taking R_{s1}, R_{s2}, R_{leak}, and C_{int} into account, one can derive an expression for electron field-effect mobility μ_{FE} (Ref. 4)

$$\mu_{\mathrm{FE}} = \frac{L_G^2 V_{\mathrm{DS}}^0 (1 + C_{\mathrm{int}}/C_{\mathrm{acc}})/C_{\mathrm{ox}}}{[(V_{\mathrm{DS}}^0 - V_s)^2/g_m^0 - V_s^2 R_{s2} - V_{\mathrm{DS}}^0 R_{s2}(V_{\mathrm{DS}}^0 - 2V_s)]}, \quad (1)$$

where L_G is the gate length, V_{DS}^0 is the applied source-drain voltage, C is the oxide capacitance, g_m^0 is the extrinsic transconductance, and V_s is the voltage drop across R_{s1} and R_{s2}. Note that if the interface states and the parasitic resistances are neglected, Eq. (1) simplifies to the usual expression $\mu_{\mathrm{FE}} = g_m L_G^2 / C V_{\mathrm{DS}}$ for the NW field-effect mobility, which leads to underestimated mobility values.[4]

The effects of interface states are further illustrated in Figs. 1(b)–1(d). Figure 1(b) shows the conduction band profile at the center of the NW channel obtained from two-dimensional Silvaco ATLAS simulation for a material stack similar to that of the InAs NWFET with V_{DS}=0.5 V and V_{GS}=−4 V. The donor-type trap levels[15] lead to the formation of an accumulation layer at the surface of InAs that alters the charge balance between the gate and NWFET channel. In the off-state biasing regime, where interface traps retain their negative charge character, the depletion region does not penetrate effectively into the NW channel. If the interface traps are allowed to neutralize (when the gate voltage hold time is close to the detrapping time constant), the gate field penetrates deeper into the NW channel and the depletion width widens. This charge balance model, shown

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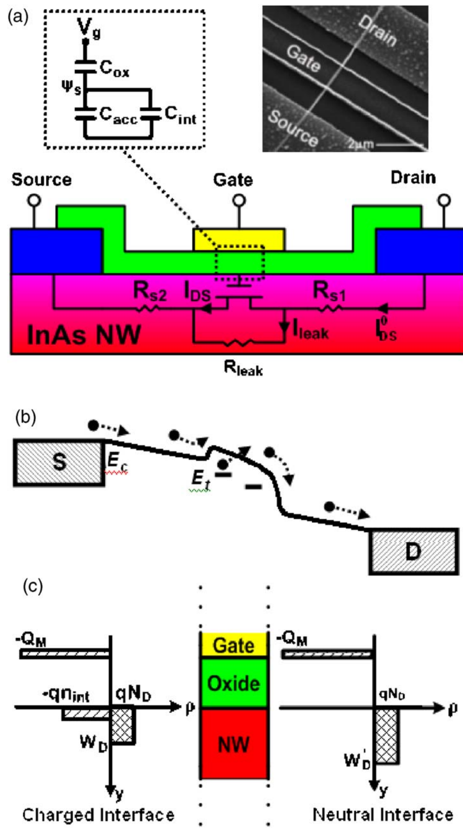

FIG. 1. (Color online) (a) Schematic diagram of the top-gated InAs NWFET with its dc equivalent circuit. Top left inset is the equivalent capacitance circuit model for the InAs NWFET including the interface capacitance C_{int}. Top right inset is a representative field emission scanning electron microscope image of the top-gate InAs NWFET. (b) E_c band-edge profile along the center of the NW channel with $V_{DS}=0.5$ V and $V_{GS}=-4$ V, including interface traps that can detrap electrons for long gate voltage hold time. (c) Charge density distribution upon negative applied V_{GS} when interface states are charged, or charge neutral leading to wider depletion depths into the channel.

in Fig. 1(c), accounts well for our experimental observations.

Figure 2 shows sweep-rate-dependent transfer characteristics obtained from an InAs NWFET at $V_{DS}=0.5$ V (the sweep direction is from negative to positive gate voltages). First, at the lowest sweep rates, I_{DS} exhibits a decay at negative V_{GS} in the off region prior to reaching I_{off} (lowest I_{DS} value). Once V_{GS} is above the threshold voltage, the gate transconductance overcomes the I_{DS} transient decay and the current increases. This unusual property in the transfer characteristics has not been discussed in the literature. These "tails" in I_{DS}-V_{GS} in Fig. 2 can be attributed to changes in

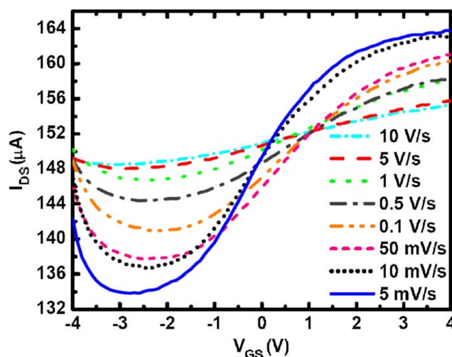

FIG. 2. (Color online) Transfer curves of an InAs NWFET with different V_{GS} sweep rates.

TABLE I. Apparent carrier mobility and concentration estimated from measurement with different gate sweep rates.

V_{GS} sweep rate (V/s)	Apparent carrier concentration n (cm^{-3})	Apparent carrier mobility μ_{FE} (cm^2/V s)
1000	9.20×10^{17}	1 270
100	8.22×10^{17}	1 415
10	7.21×10^{17}	1 665
1	5.40×10^{17}	3 230
0.1	4.62×10^{17}	6 435
0.01	4.70×10^{17}	10 665
0.001 67	4.13×10^{17}	15 980

surface state charge that are apparent when the sampling time is comparable to or longer than the characteristic time constant of surface traps. Second, the slope of the transfer curves increases with reduced sweep rates. Slow sweep rates allow surface states to attain charge neutrality and thus minimize C_{int}, which results in higher transconductance values (1 μS for 10^3 V/s and 12 μS for 1.7 mV/s). Correspondingly, the apparent μ_{FE} increases as the sweep rate is reduced. Table I summarizes the apparent mobility values obtained from Eq. (1) without considering the interface state effects, i.e., with $C_{int}/C_{acc}=0$. These results indicate that NW parameters extracted from FET characteristics may not represent the intrinsic values, but instead are highly dependent on measurement conditions. Measurements with low sweep rates (i.e., reduced C_{int}) are expected to yield transport parameters that are close to the intrinsic values of the InAs NWs. Moreover, the high field-effect mobility values confirm the potential of InAs NWs with proper surface passivation for high speed electronic applications.

The interface states also affect the estimate of mobile carrier concentration in the channel, which is given by $n_{channel}=I_{DS}L_G/q\mu_{FE}V_{DS}A$, where μ_{FE} is obtained from Eq. (1). The total carrier concentration in the channel decreases as the V_{GS} sweep rate is reduced, which is evident in the lower I_{off} values at negative V_{GS} as shown in Fig. 2. Also summarized in Table I are the computed carrier densities for this NWFET, measured with different V_{GS} sweep rates. Note that the effect of interface state charge on $n_{channel}$ is different from those observed in GaN/AlGaN based heterojunction FETs, where the interface state charges in the gate-drain extension act as a surface virtual gate and cause further depletion of the channel and $n_{channel}$ can be restored with proper passivation.[16] In these NWFETs, the interface state charges reduce the gate field and depletion width in the partially depleted NW channel underneath the gate.[4]

In order to quantify the characteristics of the interface states, we performed time resolved transfer measurements of these InAs NWFETs plotted in Fig. 3, which clearly show transient characteristics we attribute to surface state trapping and detrapping. $V_{DS}^0=0.5$ V was applied across the NWFET, and the current I_{DS} was monitored while V_{GS} was switched every 150 s in the following sequence: $0,-4,0,+4,0,\ldots,-1,0,+1,0$ V. Long characteristic time constants up to 45 s were obtained from stretched exponential fittings to $I_{DS}(t)$ decays.[17] Only transients for $V_{GS}<0$ are shown in Fig. 3 for clarity. Figure 4 shows I_{DS}-V_{GS} measurements for the same device obtained with different sweep rates. The dashed lines show I_{DS} when V_{GS} is swept with a rate of >10 V/s, for which hysteresis is clearly observed, and the solid lines in-

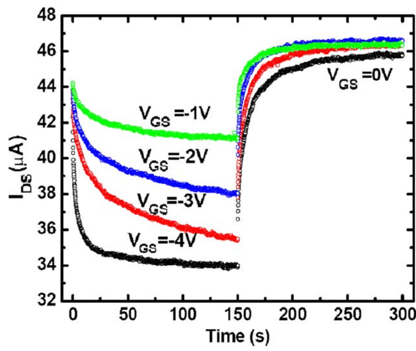

FIG. 3. (Color online) Time resolved transfer characteristics of an InAs NWFET device.

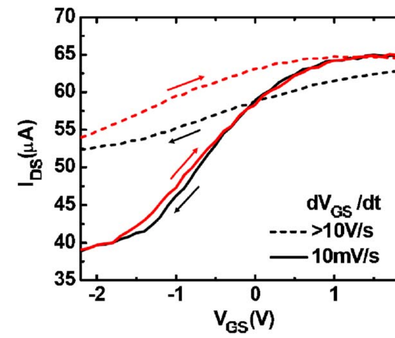

FIG. 4. (Color online) Transfer characteristics of an InAs NWFET device showing hysteresis with fast gate voltage sweep rate (dashed lines, >10V/s) and slow sweep rate (solid lines, 6.7 mV/s).

dicate transfer characteristics with a sweep rate of 6.7 mV/s, for which hysteresis is dramatically reduced. Besides the effect on hysteresis, there also exists a pronounced difference in the current level at negative V_{GS} for measurements with different sweep rates. The current level for the slow sweep rate is lower than that with the faster sweep rate which agrees well with the charge balance model depicted in Fig. 1. For slower sweep rates, the interface states are quasineutral and the depletion width extends deeper into the channel. As a result, the leakage path under the gate is reduced and the off-state I_{DS} drops.

Using the equivalent capacitance model shown in Fig. 1, one can also estimate the density of interface states ($n_{it} = C_{int}/q$, where q is the fundamental charge constant) from straightforward circuit analysis:

$$\frac{Q_{acc}}{A} = C_{acc}\Psi_s = \frac{C_{ox}}{1 + C_{int}/C_{acc} + C_{ox}/C_{acc}}(V_{GS} - V_t), \qquad (2)$$

where Ψ_s is the surface potential at the oxide-InAs interface, A is the effective NW surface area under the gate, and V_t is the threshold voltage. C_{ox}/C_{acc} is negligible due to the large oxide thickness as compared to the small spatial separation between the accumulation charges and the interface. Note that any bulk traps contribute to a much smaller capacitance and are thus excluded from Eq. (2). In Fig 4, when a slow sweep rate of 6.7 mV/s was used, the hysteresis was diminished, indicating that the interface states are quasineutral; i.e., the interface state capacitance C_{int} is negligible and can be eliminated from Eq. (2), and the intrinsic transconductance (g_m) can be calculated from the extracted I_{DS}-V_{GS} by applying circuit analysis techniques to the dc equivalent circuit in Fig. 1. The ratio of the transconductance of the NWFET with neutralized interface states (g_{m1}) to that with surface charges (g_{m2}) then obeys the relationship

$$1 + C_{int}/C_{acc} = g_{m1}/g_{m2}. \qquad (3)$$

Assuming that the interface states are neutral for the gate sweep with 6.7 mV/s in Fig. 4, g_{m1}/g_{m2}=35 μS/15 μS =2.3. If a ~10 nm separation between the accumulation layer and the InAs/oxide interface is assumed (from one-dimensional Schrödinger-Poisson solution), the interface state capacitance can be calculated from Eq. (3) to be ~2 μF/cm^2. This value corresponds to an interface state density of $\sim 4 \times 10^{12}$ cm^{-2} by assuming the traps to be uniformly distributed over 0.34 eV ($\sim E_g$) for InAs, which agrees well with values used to fit experimental data in similar InAs NWFETs.[18]

In summary, we have fabricated InAs NWFETs and investigated the capacitive effects of surface states on the FET transport properties. The InAs NWFETs exhibited transient behavior that severely affects characteristic NW parameter extraction. From circuit and device analyses, we obtain apparent field-effect mobility values in the range of 1000–16 000 cm^2/V s and surface state density in the low 10^{12} cm^{-2} range. The upper end of the mobility range is believed to best reflect the values intrinsic to transport within the NW. This analysis may help explain the wide range of NW parameters reported in the literature, which indicates that measurements with a charge neutralized (or passivated) surface allow the extraction of the intrinsic nanowire transport parameters, and highlights the potential of InAs NWs for high speed electronics with effective surface passivation.

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